Design of 4-bit Barrel Shifter in Quantum Dot Cellular Automata

by

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Declaration

I hereby declare that

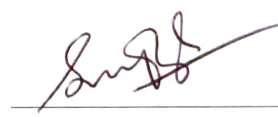
i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology and has not been submitted elsewhere for a degree,

ii) due acknowledgment has been made in the text to all the reference material used.

KOLLIPARA SAI SREE ROHINI

Certificate

This is to certify that the thesis work entitled DESIGN OF 4-BIT BARREL SHIFTER IN QUANTUM DOT CELLULAR AUTOMATA has been carried out by KOLLIPARA SAI SREE ROHINI for the degree of Master of Technology in Information and Communication Technology at *Dhirubhai Ambani Institute of Information and Communication Technology* under my/our supervision.



Prof. SREEJA RAJENDRAN
Thesis Supervisor

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I would like to express my sincere gratitude to Prof. Sreeja Rajendran, whose knowledge was crucial in defining the problem statement and exploring the techniques involved in the chosen field of study. Her incisive feedback and guidance pushed me to sharpen my thinking and improve the calibre of my work.

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Contents

Abstract

This thesis proposes the design of a 4-bit barrel shifter using Quantum Dot Cellular Automata (QCA) technology. With decreasing feature size, CMOS technology faces various challenges like leakage current, drain induced barrier lowering, power dissipation etc. Researchers have proposed alternative technologies which helps to alleviate the problems associated with CMOS. Quantum Dot Cellular Automata (QCA) is one such promising technology which can replace transistor based CMOS Technology. The thesis begins with an introduction to QCA technology and its basic elements which are QCA inverter and QCA majority gate. Basic logic gates designs are implemented using majority gates and inverter. It then presents two major concepts of QCA namely QCA Clocking and QCA Crossover. QCA Clocking is a technique used to synchronize QCA cells, while QCA Crossover is used to transmit signals through crossing wires. The crux of the thesis is the design of a 4-bit barrel shifter using QCA technology. Barrel shifter is a crucial component in digital signal processing and graphics applications. The left and right shift operations of barrel shifter are useful in finding Greatest Common Divisor(GCD) using Steins' Algorithm. The proposed design is a right shifter that is capable of shifting the input by one, two, or three positions to the right, depending on the control signals.The proposed design utilizes optimized 2:1 multiplexers which provide the advantage of minimum area and power consumption. The proposed design is simulated using QCADesignerE software, and the obtained results are compared with the performance of existing shifters in QCA.The simulation results demonstrate that the proposed design provides a significant improvement in terms of area with a cell count of 381 and a delay of 6 clock phases. Further, a comparison of the proposed QCA based barrel shifter with conventional CMOS-based shifter is also presented.

List of Principal Symbols and Acronyms

ρ	Electric charge
GCD	Greatest Common Divisor
MUX	Multiplexer
QCA	Quantum-dot Cellular Automata

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CHAPTER 1
Introduction

1.1 Motivation

Modern computing devices like personal computers, smartphones, and video game consoles primarily rely on processors built using metal-oxide semiconductor field effect transistors (MOSFETs). Over the past few decades, MOSFETs have significantly reduced in size, from micrometers in the 1960s to nanometers today [1]. This miniaturization has led to faster chip performance and lower power consumption. As a result, MOSFET-based architectures have found applications in various fields. However, it is widely believed that current MOSFET-based circuits are nearing their performance limits. With technology scaling beyond 17nm, MOSFET performance is dominated by second order effects like leakage currents, power dissipation etc [2].

1.2 Alternatives to MOSFET

Due to the limitations of MOSFETs, researchers have actively pursued alternatives. A comprehensive exploration of alternative state variables for emerging nanolectronic devices is discussed in [3]. Two main approaches have been adopted by research groups. The first approach focuses on developing new transistor-based devices, such as the tunnel FET, single electron transistor, and carbon nanotube FET, to address the limitations. The second approach involves exploring alternatives to transistor-based devices. This category includes spin-wave devices and quantum dot cellular automata.

1.3 Why QCA?

Quantum Dot Cellular Automata is an evolving alternative technology which has the potential to replace CMOS based devices. It has several advantages such as high density, high speed, low size and low power consumption [4], [5]. QCA offers the ability to create smaller electronic devices with exceptionally high computation switching speed [6]. QCA technology works on the principle of cell polarization. This implies that there is no actual current flow in a QCA circuit and as a result, QCA circuits have extremely low power consumption.

1.4 Previous work

The concept of QCA was first proposed in [7],and since then, several researchers have explored its potential for future computing applications [8]. The design of inverters, 3 input majority gate and basic logic gates are presented in [9]. Researchers have explored the design of a 5-input majority gate and various such designs of majority gates are in [10–14]. XOR gate is one of the basic building blocks in digital circuits, which is useful in various arithematic operations, error detection and correction. Some of the designs of XOR gate are presented in [15–20]. The initial designs of adders in Quantum-dot Cellular Automata (QCA) utilized five majority gates and three inverters [9]. By connecting multiple one-bit QCA full adders, a carry look-ahead (CLA) adder can be constructed, enabling the generation of carry signals before calculating the sum [21]. Additionally, a novel bit-serial QCA adder has been introduced [22], which employs carry feedback and minimizes the gate count to three majority gates and two inverters. The one-bit QCA adder in [23] is built upon a novel algorithm that achieves QCA addition using only three majority gates and two inverters. In addition, the design of multiplexers has also been carried out. Multiplexer is a universal logic module as it can be used to implement any digital design. There are several designs proposed for multiplexers in [24–28] Different designs for other arithmetic modules like barrel shifters are explored in [21, 29].

1.5 Organisation of Thesis

The subsequent chapter introduces relevant QCA fundamentals that will be used throughout the thesis which include basic QCA cell and its working, QCA

wire and basic QCA elements i.e inverter and majority logic gate. Chapter 3 delves into the explanation of QCA clocking and QCA crossover concepts. Moving on to Chapter 4, it covers the design of fundamental logic gates using majority gates, full adder design, the design of a 2:1 multiplexer and the design of a 4:1 multiplexer using MUX trees. The chapter also presents the optimized design of a 2:1 MUX. Chapter 5 shifts the focus towards the operation, applications, and proposed design of a barrel shifter. The simulation and results obtained from the proposed barrel shifter are also presented in Chapter 5. Lastly, the final chapter concludes the work by discussing the findings, implications, and future scope for the proposed work.

CHAPTER 2
QCA FUNDAMENTALS

Quantum-dot Cellular Automata (QCA) is a computing paradigm based on nanotechnology that utilizes the principles of quantum mechanics for executing logical operations. It allows electrons to tunnel through potential barriers to create stable charge configurations. When a voltage is applied to the cell, the quantum dots in the cell create a potential well that captures the electrons from the neighboring cells. The tunnelling process is governed by the Schrödinger wave equation, which describes the probability of finding an electron at a given position in the potential well.

2.1 Basic QCA cell

A QCA cell consists of two electrons and four quantum dots.There are two types of QCA cells. One is standard cell and the other is rotated cell. The electrons are located in antipodal positions as a result of coloumbic interactions [5].The position of the electrons determines the polarization of the cell. Figure 2.1 depicts the two polarizations in standard cell [30] [31] [32] and Figure 2.2 shows the two polarizations of rotated cell.The polarization of a cell can be calculated by the equation below [9]:

$$P = (\rho_1 + \rho_3) - (\rho_2 + \rho_4))/(\rho_1 + \rho_2 + \rho_3 + \rho_4) \tag{2.1}$$

where ρ_i is the electric charge in the dot i.

2.2 QCA wire

QCA wire can be employed to transmit binary information between two points, as the polarization of each cell tends to align with that of its neighboring cells. [30].

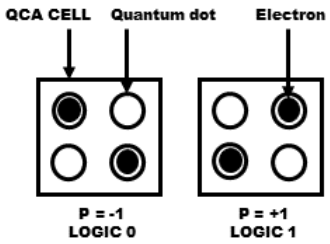


Figure 2.1: QCA standard cell with different polarizations

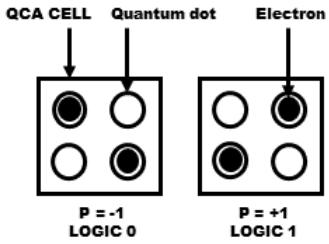


Figure 2.2: QCA rotated cell with different polarizations

A QCA wire is formed by arranging QCA standard cells linearly to form an array. The information is transferred as a result of the coloumbic interactions between the electrons. The output of wire depends on the type of cell and cell count between input and output. A QCA wire is said to be ideal if it contains atleast two cells in each clock zone. Binary information can also be transferred using QCA rotated cells. As the neighbouring rotated cells tend to have opposite polarization, even number of rotated cells can be used to transmit data [33].The binary 90° wire and 45° wire is shown in Figure 2.3. For the research work carried out, binary 90 degree wire structure is used [34] [35] [36].

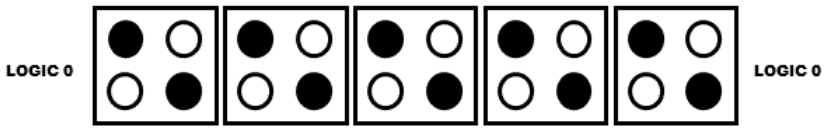
2.3 Basic QCA elements

Majority gates and inverters are referred to as basic QCA elements [9], [37]. Employing a combination of majority gates and inverters, any Boolean logic can be implemented. In addition to these, it is also possible to realize any logic function using multiplexers (Universal logic module) and a look up table [17].

2.3.1 Inverter

Two standard cells in a diagonal orientation are geometrically similar to two

(a)



(b)

Figure 2.3: (a) 90° wire, (b) 45° wire,

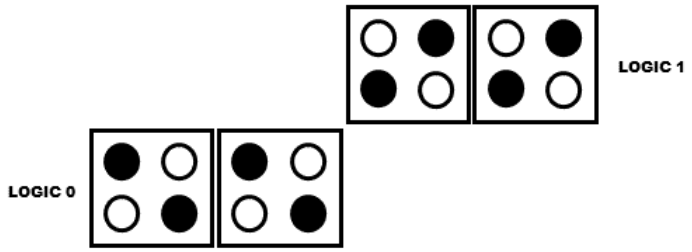
rotated cells in a horizontal orientation. If the input of the inverter gate changes to logic 0, the output changes to logic 1, and vice versa [9]. As shown in Figure 2.4(a), QCA inverter is formed by aligning two QCA cells diagonally. The inversion of electrostatic interaction occurs due to the misalignment of quantum dots with different polarizations between the cells [6]. In Figure 2.4(b), alternative inverter design called double path inverter or robust inverter is also shown. The data in a cell will be inverted if the dots within it are rotated 45 degrees. These 45° cells will result in the formation of a inversion chain or a wire where each cell has the opposite polarity of its close neighbours. Inversion chain is demonstrated in Figure 2.4(c).

2.3.2 Majority gate

A majority gate is a configuration of five standard cells shown in Figure 2.5(a). The centre cell is referred to as the device cell, while the three cells at the top, bottom, and left function as inputs. The right cell serves as an output. The output of the gate is determined by the device cell or decision cell [9]. The majority among the inputs determines the output of the majority gate. Figure 2.5(b) depicts this new logic gate in representation. In terms of a boolean function, majority logic can be described as follow:

$$M(A, B, C) = AB + BC + AC \tag{2.2}$$

(a)



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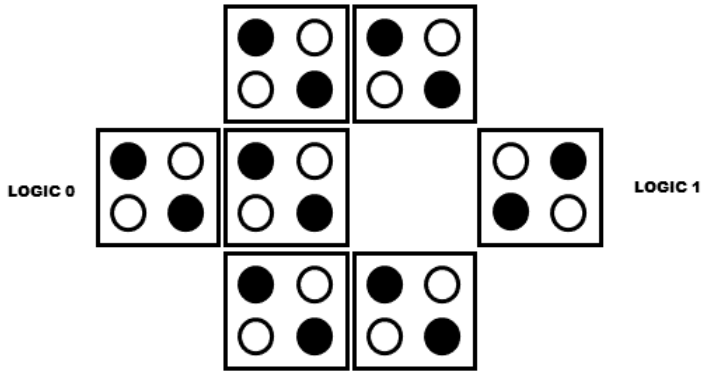

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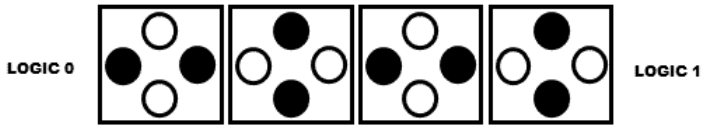
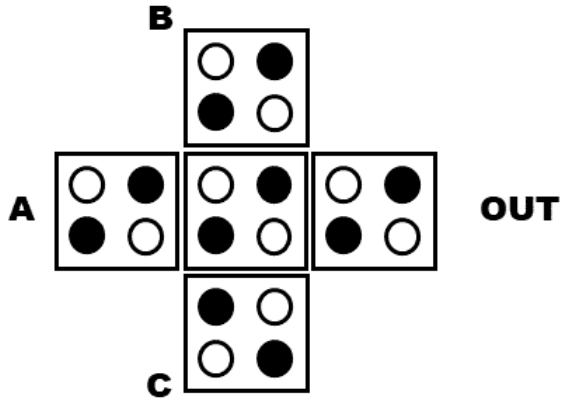


Figure 2.4: (a) Simple inverter (b) Robust inverter (c) Simple inverter using rotated cells

(a)



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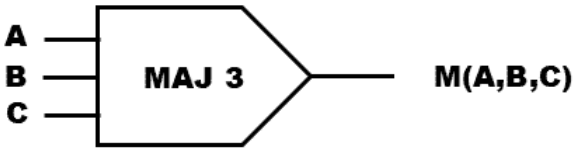


Figure 2.5: (a) QCA majority gate (b) Schematic of majority gate

Researchers have designed a majority gate with 5 inputs to develop more optimised circuits. This gate has 5 inputs A,B,C,D and E. The boolean expression for the 5-input majority gate is depicted in (2.3). There are many proposed designs of QCA 5-input majority gate. The first design of 5-input majority gate is presented in Figure 2.6(a) [10]. It has 11 QCA cells and the drawback of this design is that it is not feasible to simultaneously access both input cells A and C within a single layer. In the second design presented in [11], as illustrated in Figure 2.6(b), has 10 QCA cells. The output cell in this design is enclosed by the adjacent cells. The other designs are shown in Figure 2.6(c) - Figure 2.6(f).

$$\begin{aligned} M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE \\ + ADE + BCD + BCE + BDE + CDE \end{aligned} \tag{2.3}$$

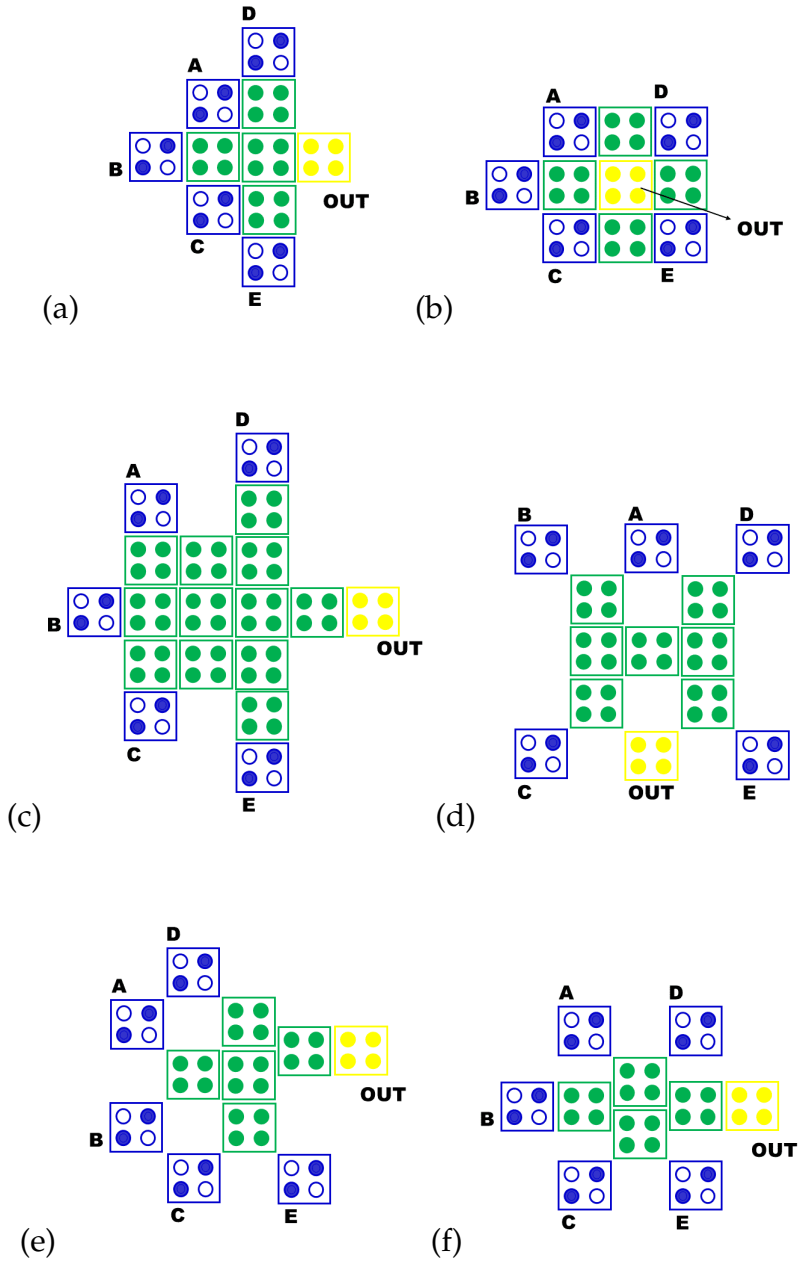


Figure 2.6: Designs of existing 5-input majority gates (a) in [10], (b) in [11], (c) in [12], (d) in [13], (e) in [14], (f) in [38]

CHAPTER 3
QCA Clocking and QCA wire crossing

3.1 QCA Clocking and Types

Clocking plays a vital role in both sequential and combinational circuit designs in QCA. Timing of signals is controlled through clocking. It facilitates the transfer of information from one end of a wire to the opposite end. Similar to the power loss in electric transmission systems, there is inevitable signal degradation during the transmission of QCA signals.

To prevent information loss, the signal needs to be periodically restored during the transmission process [6]. In QCA design, this restoration is achieved through the application of a clock, which provides the necessary energy without the flow of current. By applying a clock to the QCA cells, each stage gains actual power, enhancing weak input signals and restoring logic levels. Consequently, the accuracy of the signal is preserved, ensuring reliable signal transmission [39]. Zone clocking and continuous clocking are the two types of clocking. Because continuous clocking is not supported by QCA tools, we only adhere to zone clocking. Zone clocking consists of four phases [40]: switch, hold, release, and rest as shown in Figure 3.1.

During the switch phase, the interdot barriers of the cells are gradually lowered, eliminating the previous polarizations induced by the old input [41]. By the end of this phase, the cells exhibit minimal or no polarization. In the subsequent hold phase, the interdot barriers are raised while applying the new input. This increase in interdot barriers prompts the cells to repolarize, adopting well-defined bistable states that correspond to the new inputs and reach the ground state [41]. In the release phase, the barriers are dropped, and during the relax phase, they remain lowered and unpolarized. The four-phase clocking scheme is depicted in Figure 3.2. Figure 3.3, depicts the operation of QCA wire in different clock zones.

Initially, the cells in clock zone 0 are in switch phase and so they get polarized according to the polarization of input cell. In the next phase, the cells in clock zone

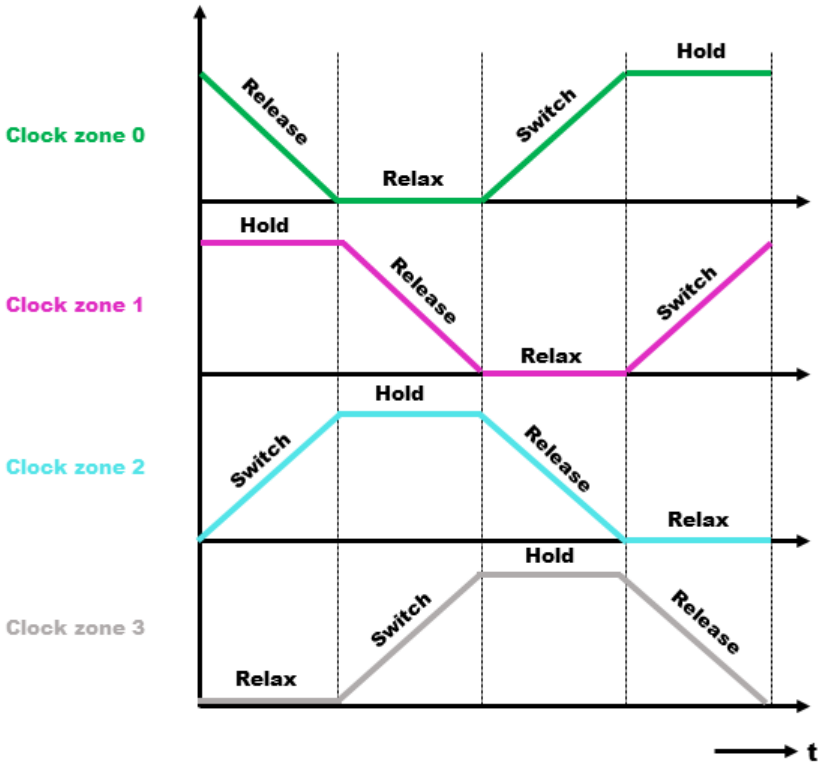


Figure 3.1: QCA clock zones

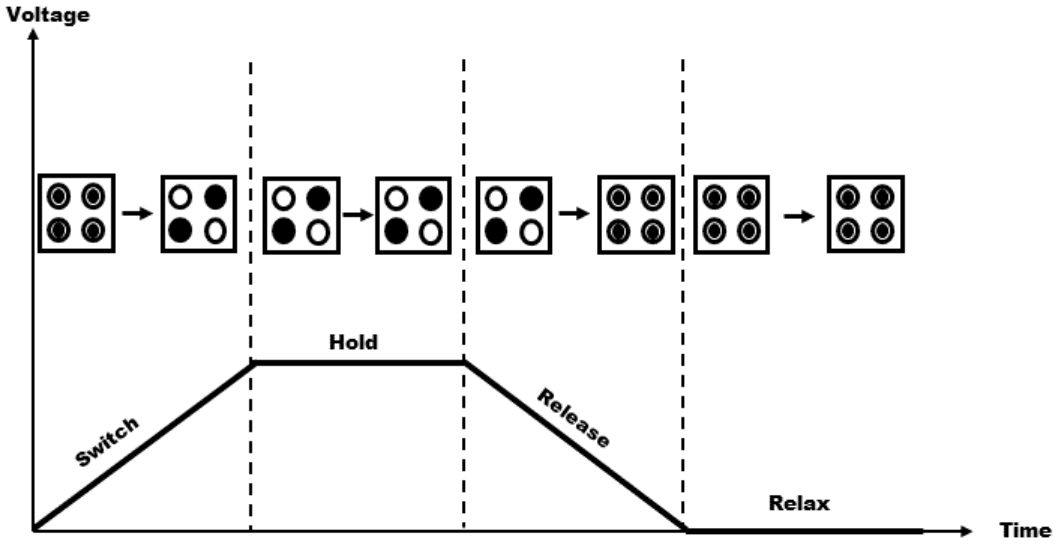


Figure 3.2: QCA clocking scheme

0 will be in hold phase and the cells in clock zone 1 will be in switch phase. When clock zone 2 gets into switch phase, the clock zone 0 will be in release phase. At the last, the clock zone 3 will be in switch phase, clock zone 2 in hold phase, clock zone 1 in release phase and clock zone 0 wil be in relax phase so that the cells will be ready to get new polarization of input.

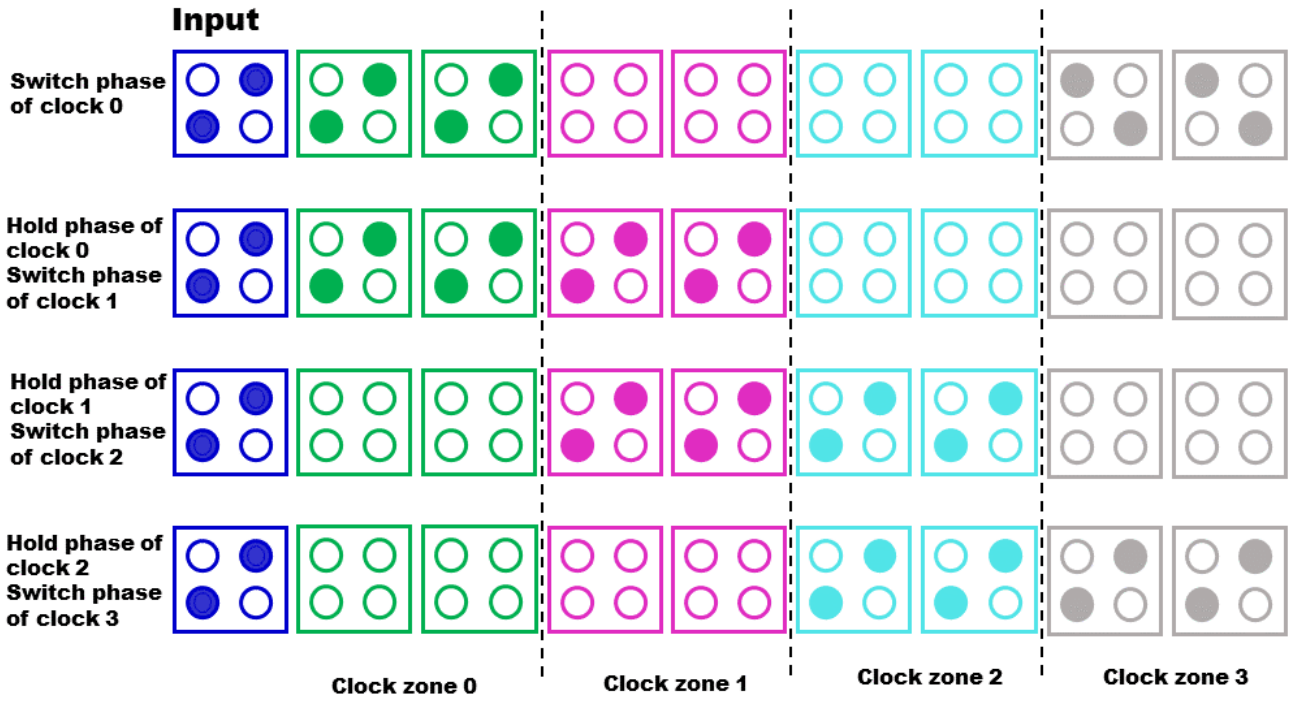


Figure 3.3: Operation of wire in different clock zones

Figure 3.4 is the layout of a QCA wire which has different clock zones. There will be a difference of 90° in the phase of input in each clock zone. The phase difference with respect to each clock zone is illustrated in Figure 3.5.

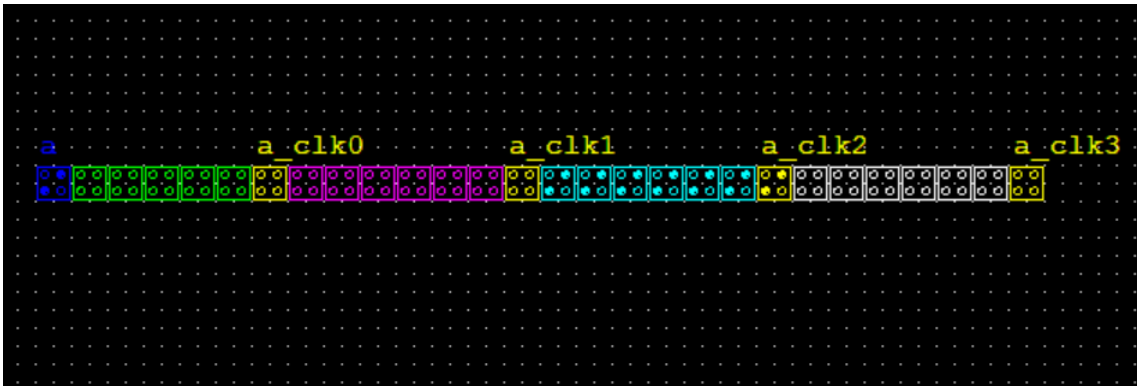
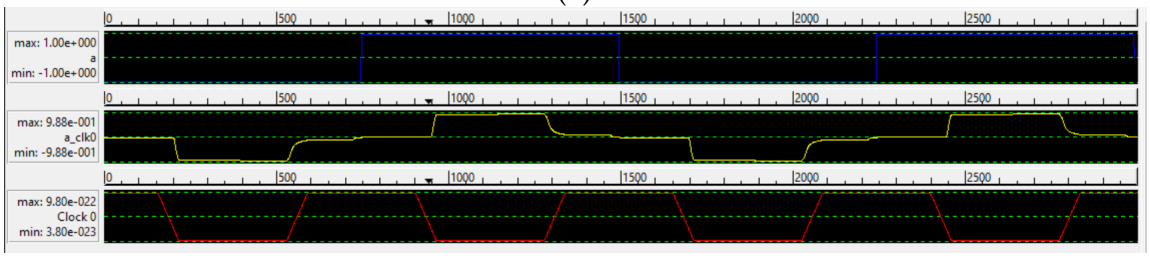


Figure 3.4: QCA layout of a wire with different clock zones

(a)



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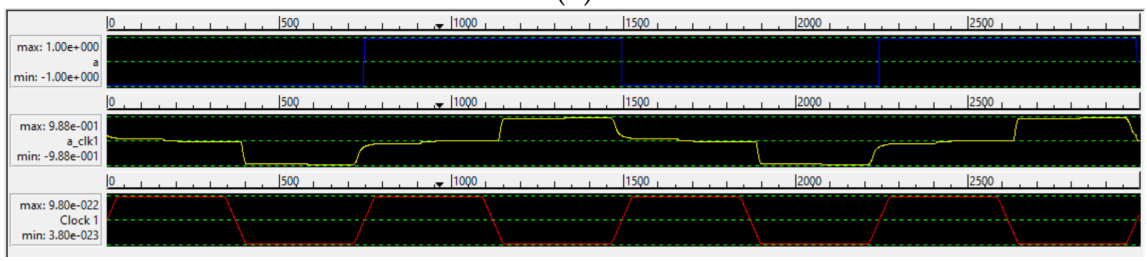

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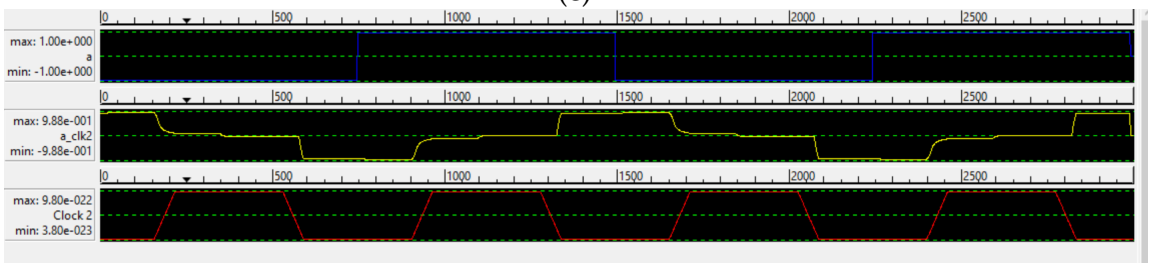


(d)

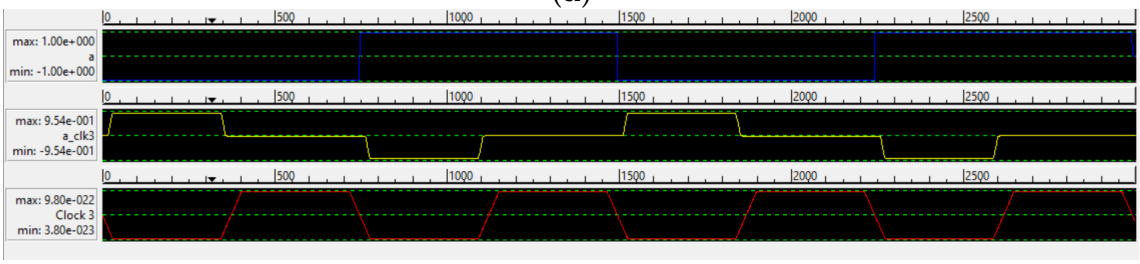


Figure 3.5: (a) Output of wire in clock zone 0 (b) Output of wire in clock zone 1 (c) Output of wire in clock zone 2 (d) Output of wire in clock zone 3

3.2 QCA wire crossings

While designing circuits in QCA, there arises the need for one or more signals to cross over existing cells to reach fan-out branches. In order to make this possible, there are wire crossing techniques available in QCA technology. Three prominent techniques for wire-crossing in QCA circuits are the coplanar-based, multilayer-based, and clocking-based.

Coplanar-based wire-crossing technique introduced in [9], is illustrated in Figure 3.6(a), where vertical wires transmit the value '0' and horizontal wires transmit the value '1'. To implement this wire-crossing, the cells of the vertical wire are rotated by a certain angle. In order that the transmitting value is not affected by the horizontal wire, it is necessary to have at least three cells after the intersection with the horizontal wire. Notably, the vertical wire in the proposed wire-crossing technique should have an odd number of cells. This requirement arises from the characteristic of the rotated cells, which introduces additional spacing between the cells. This spacing affects the energy separation between the ground state and the first excited state, impacting the device's performance in terms of maximum operating temperature, resistance to entropy, and minimum switching time [42].

The multilayer-based wire-crossing technique employs a crossover bridge method, which resembles the appearance of two wires crossing each other. In reality, it utilizes a stereoscopic structure, as depicted in Figure 3.6(b). In this technique, the horizontal chain incorporates a crossover bridge. Compared to the coplanar-based technique, this approach offers greater potential for miniaturization and generalization since it does not require cell rotation. It is worth mentioning that the multilayer-based wire-crossing technique may experience challenges related to noise in the crossover area between the intersecting cells [43].

In switch and release phases, there exist duplicated states between the ground and excited because tunneling barriers of each stage are still raising and lowering, respectively. The hold and relax phases have a fixed state such as a ground state or an excited state. Because tunneling barriers of these phases are completely raised and lowered, respectively. If two adjacent cells have different clock zones at the same time and each clock zone has the switch and hold phases pair, data transmission is performed within two cells. When a cell in the hold stage maintains a fixed polarization value, the adjacent cell in the switch state also adopts the same polarization value. This is due to the Coulomb repulsion between the two cells and the transition from an excited state to a ground state.
On the contrary, if each clock zone for two adjacent cells has the hold and release

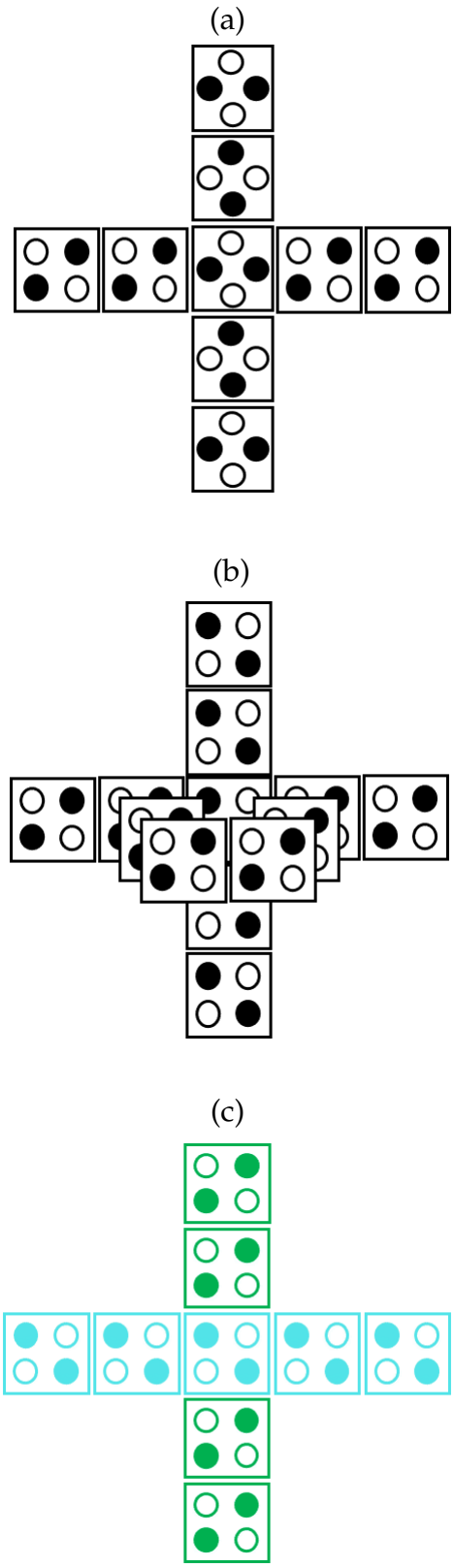


Figure 3.6: (a) Coplanar crossing (b) Multilayer crossing (c) Crossing with different clock zones

stages, the switch and relax phases or the switch and release stages, data transmission does not operated within two cells. This is because each clock zone is transformed to a different state. If each clock zone of two(adjacent cells is the hold and relax phases pair, meantime, they have different states (that is, ground and excited states) and there does not exist the Coulomb repulsion between the two cells. So, data transmission is performed without any interference. As depicted in Figure 3.6(c), when two adjacent pairs have clock zones 0 and 2, they can successfully perform the wire-crossing without any interference. Similarly, if two adjacent cells have a clock zone 1 and 3 pair, they can also execute the wire-crossing without encountering interference.

CHAPTER 4
Design of Basic Digital Circuits in QCA

4.1 Design of Basic logic gates using majority gate and inverter

The logic function for the three-input majority gate, which has inputs A, B, and C, is represented by M(A, B, C) = AB + BC + CA. By utilizing this function, we can implement a two-input AND gate as M(A, B, 0).

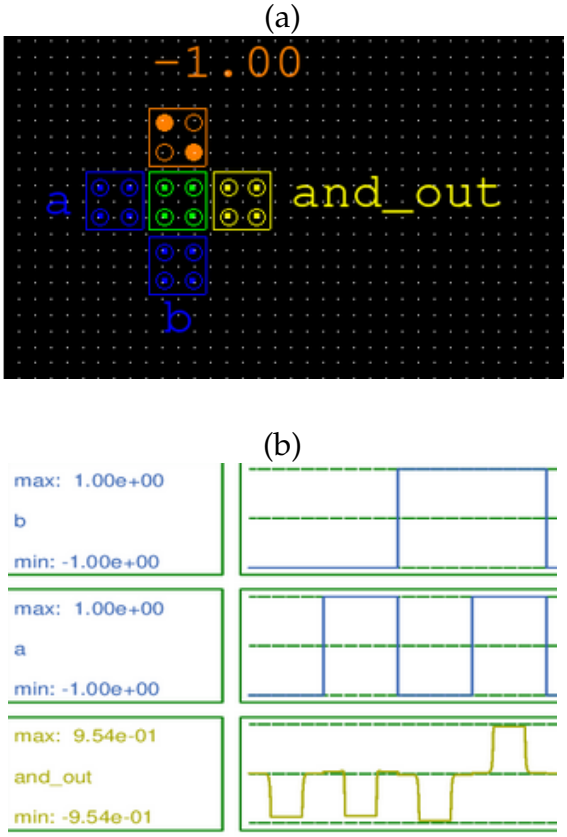
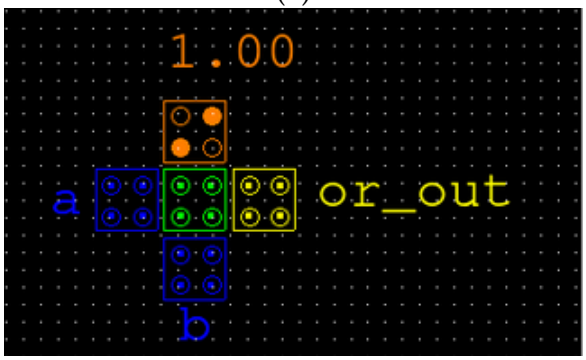


Figure 4.1: (a) Layout of AND gate (b) Simulation results of AND gate

The QCADesignerE layout for the 2-input AND gate is illustrated in Figure 4.1(a). In QCADesigner terminology, the input C for a 2-input AND gate is as-

(a)



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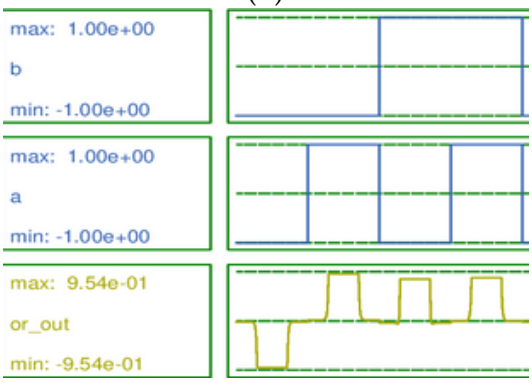
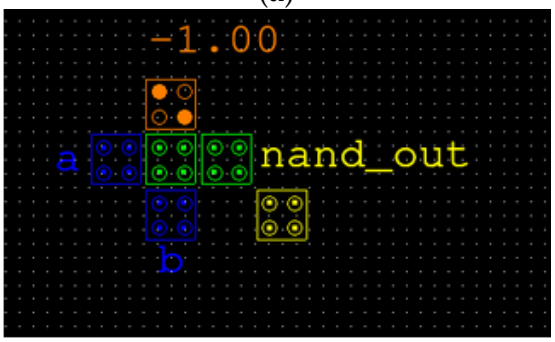


Figure 4.2: (a) Layout of OR gate (b) Simulation results of OR gate

signed a fixed polarization value of -1.0. When designing the layout, it is also necessary to specify the appropriate clock zones to the QCA cells. In this particular case, all the cells are set to clock zone 0. As a rule, all the inputs to a circuit are required to be set to clock zone 0.

Figure 4.1(b) illustrates the simulation results of a 2-input AND gate implemented in QCADesignerE.The implementation of the OR operation of two inputs A and B is achieved by setting the third input C to 1, resulting in A+B. The layout design for a 2-input OR gate is presented in Figure 4.2(a), and the corresponding simulation results can be observed in Figure 4.2(b). The implementation of a two-input NAND gate and a two-input NOR gate in QCA involves utilizing one majority gate followed by one inverter for each gate. The layouts for the 2-input NAND gate and the 2-input NOR gate can be seen in Figures 4.3(a) and 4.4(a) , respectively. The corresponding waveforms depicting the behavior of these gates are displayed in Figures 4.3(b) and 4.4(b), respectively.

(a)



(b)

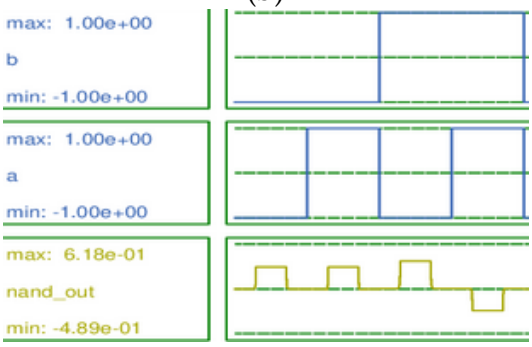
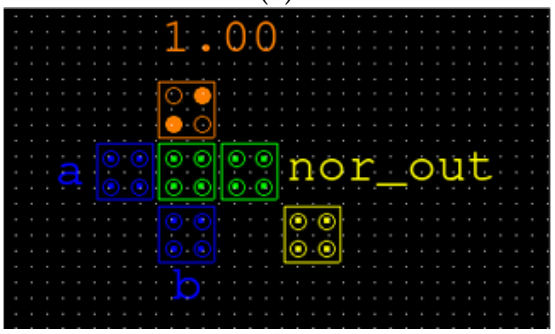


Figure 4.3: (a) Layout of NAND gate (b) Simulation results of NAND gate

(a)



(b)

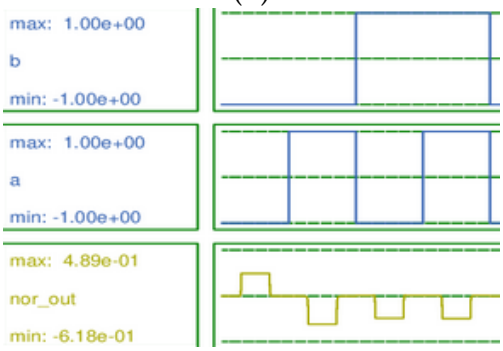


Figure 4.4: (a) Layout of NOR gate (b) Simulation results of NOR gate

4.2 Design of 2:1 multiplexer

Multiplexer is a logic module that finds applications in various logic designs. It can be used to implement any logic function like adders, shifters etc. Figure 4.5 illustrates a 2-to-1 multiplexer, which implements the logic function C = AS + BS'. This design requires the utilization of three majority gates and one inverter. The simulation results for the multiplexer can be observed in Figure 4.6(b). It has a cell count of 39 and occupies an area of 0.05 μm^2.

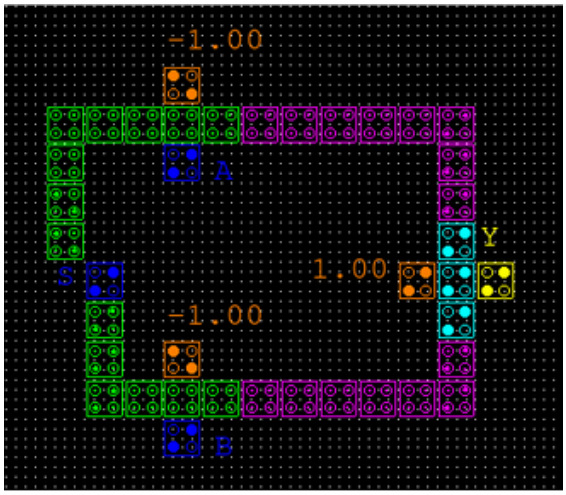
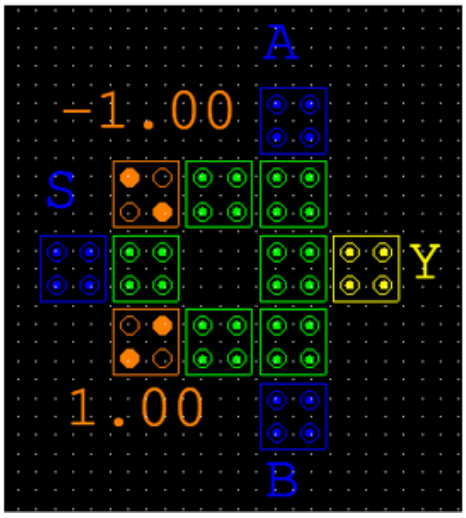


Figure 4.5: Layout of 2:1 Multiplexer

4.3 Design of optimized 2:1 multiplexer

The structure of this component is straightforward, highly efficient, and offers significant utility in implementing various logical functions. It does not adhere to any specific Boolean function but instead leverages the inherent characteristics of quantum technology to generate the desired output. It consists of 12 cells, 1 clock zone delay and no cross wiring [44]. Layout and simulation results of the optimized multiplexer are depicted in Figure 4.6(a) and (b). It occupies an area of 0.01 μm^2.

(a)



(b)

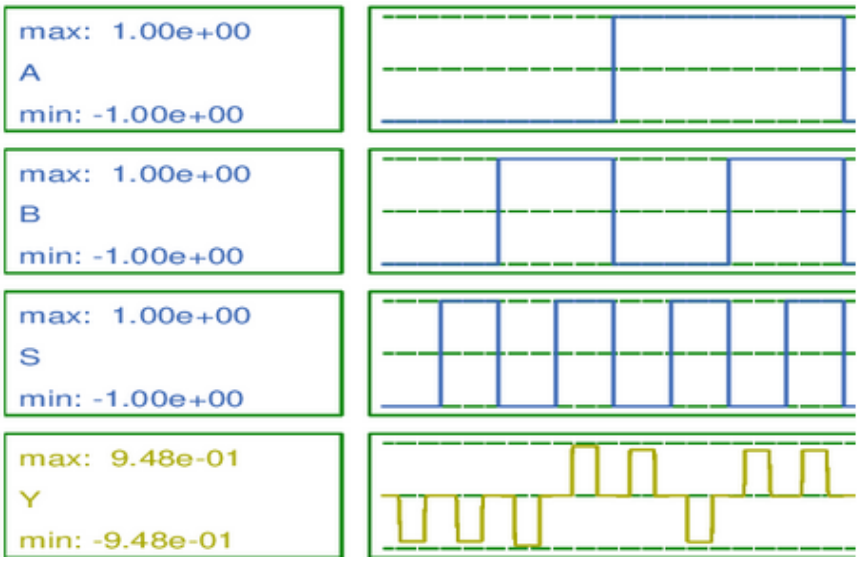
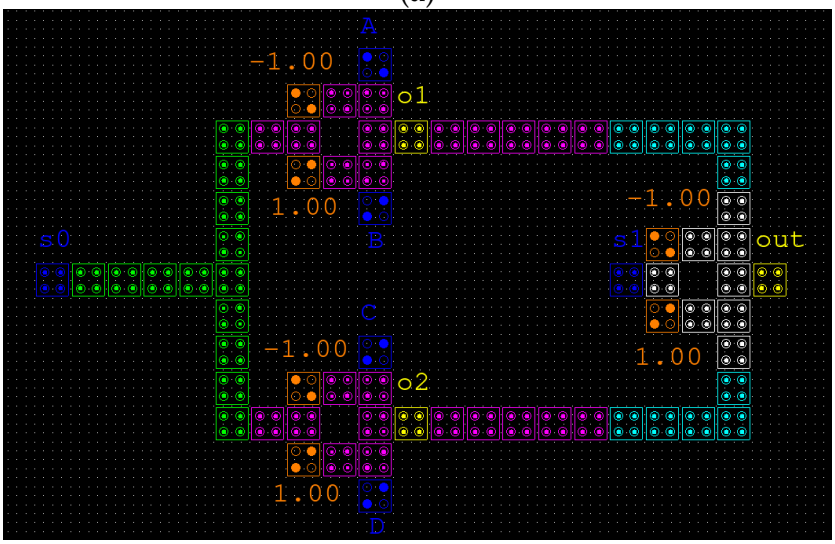


Figure 4.6: (a) Layout of optimized 2:1 Multiplexer (b) Simulation results of optimized 2:1 Multiplexer

4.4 Design of 4:1 multiplexer using 2:1 multiplexer

Using optimized 2:1 MUX which is presentes in last section , we have build a 4:1 mux. It requires 3 2:1 multiplexers. Layout and simulation results of the optimized multiplexer are depicted in Figure 4.7(a) and (b). It consists of 70 cells, 3 clock zone delay and no wire crossing. It occupies an area of 0.12 μm^2.

(a)



(b)

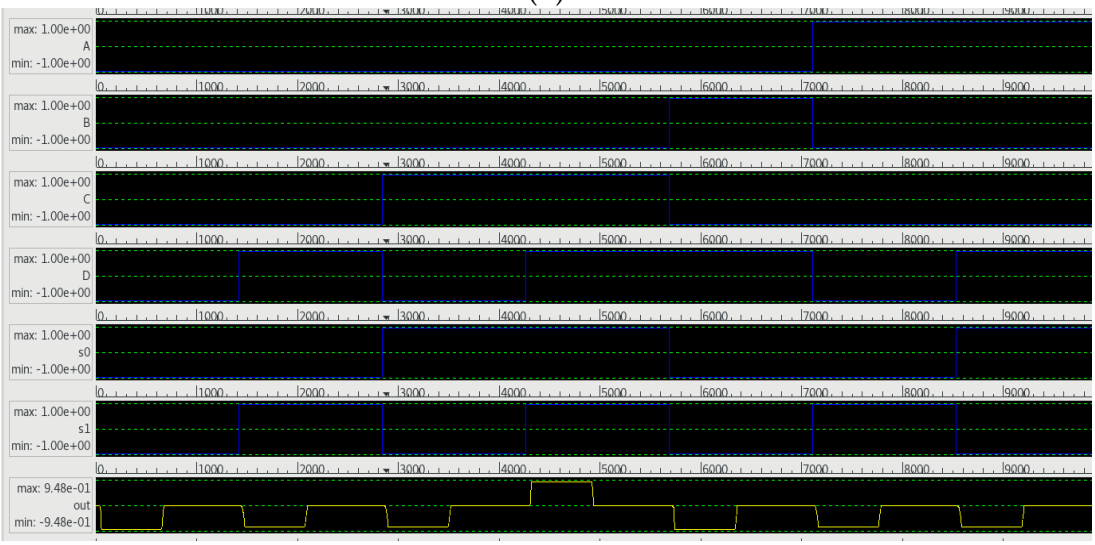
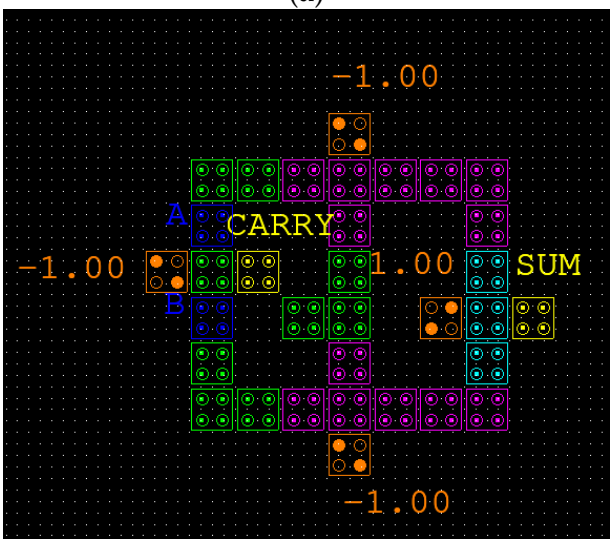


Figure 4.7: (a) Layout of 4:1 Multiplexer (b) Simulation results of 4:1 Multiplexer

4.5 Design of half adder

In this structure of half adder, we require 3 and gates, 1 or gate and 1 simple inverter. The majority gate logic is used to implement and and or gates. It requires 33 QCA cells to build this structure in QCA. It has a delay of 3 clock zones delay and it occupies an area of 0.05 μm^2.

(a)



(b)

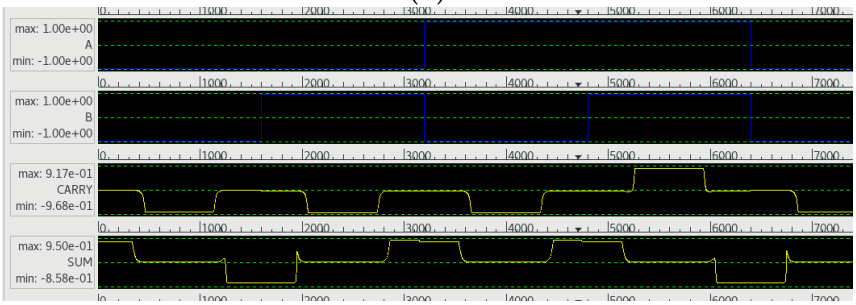


Figure 4.8: (a) Layout of Half adder (b) Simulation results of Half adder

The details of the circuits implemented in this chapter all together presented in Table 4.1. It includes cell count, area and delay of the output.

Circuit	Cell count	Area	Delay
2:1 mux	39	0.05 μm^2	3 phases
Optimized 2:1 mux	12	0.01 μm^2	1 phase
4:1 mux	70	0.12 μm^2	4 phases
Half adder	33	0.05 μm^2	3 phases

Table 4.1: Cell count, area and delay of the circuits implemented

All simulations were conducted using QCADesigner v2.0.3, employing the coherence vector simulation engine. The simulation parameters utilized were the default values provided by QCADesigner, which are detailed in Table 4.2.

Parameter	Coherence vector
Cell size	18*18 nm^2
Layer seperation	11.5 nm
Spacing between quantum dots	8nm
Radius of effect	80nm
Relative permittivity	12.9
Clock high	9.8e-22 J
Clock low	3.83-23 J
Clock amplitude factor	2

Table 4.2: Coherence vector cell parameters

CHAPTER 5
Proposed Design of Barrel Shifter, its Application in Binary GCD algorithm, Simulation and Results

5.1 Design and Operation of Barrel Shifters

Barrel shifter is a logical data shifter circuit which has N inputs and N outputs. It has a set of control inputs which determines whether a shift operation will be performed on the input data or not. In left shift, a zero is inserted into the Least Significant Bit (LSB) position, and the remaining bits are moved towards left by one bit position resulting in the discard of the Most Significant Bit (MSB). On the other hand, in right shift, the LSB is discarded, a zero is inserted in MSB and the remaining bits are moved towards right by one position.

Left shift by k bit positions is equivalent to multiplication by 2^k. Likewise, right shift corresponds to division by 2^k. The decimal equivalent of control input value determines the amount of shift in the data. The left and right shift operations are demonstrated in Figure 5.1 (a) and (b).

5.2 Design of barrel shifter

A barrel shifter is constructed using an array of 2 to 1 multiplexers connected in multiple levels. The number of multiplexers in a level corresponds to the input data size. For instance, for a 4-bit number, there will be 4 multiplexers in each level.Each level has a separate select line. For an n-bit number, the maximum number of shifts possible is (n-1).

The block diagram of right shift operation of a 4-bit number using 2:1 MUX is illustrated in Figure 5.2. In the case of a 4-bit number, a shift of 2 bit positions

is enabled by the upper level and a 1-bit shift is enabled by the lower level of MUX arrays. Here A3,A2,A1,A0 are the inputs bits, S1,S0 are control inputs and Y3,Y2,Y1,Y0 are the output bits. Table 5.1 describes how the inputs are 4shifted based on the values of control inputs.

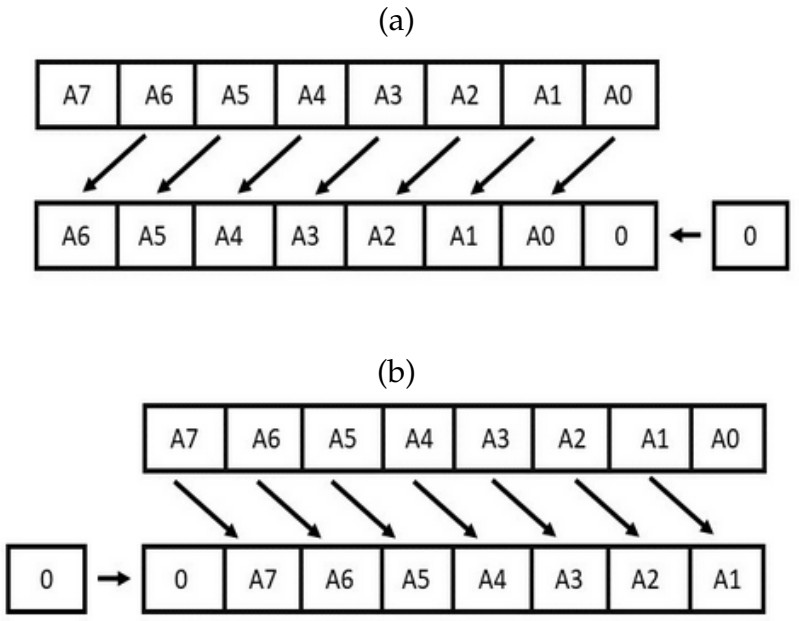


Figure 5.1: (a) Left shift operation (b) Right shift operation

S1	S0	Operation
0	0	No shift
0	1	1-bit shift
1	0	2-bit shift
1	1	3-bit shift

Table 5.1: Operational function of Barrel right shifter

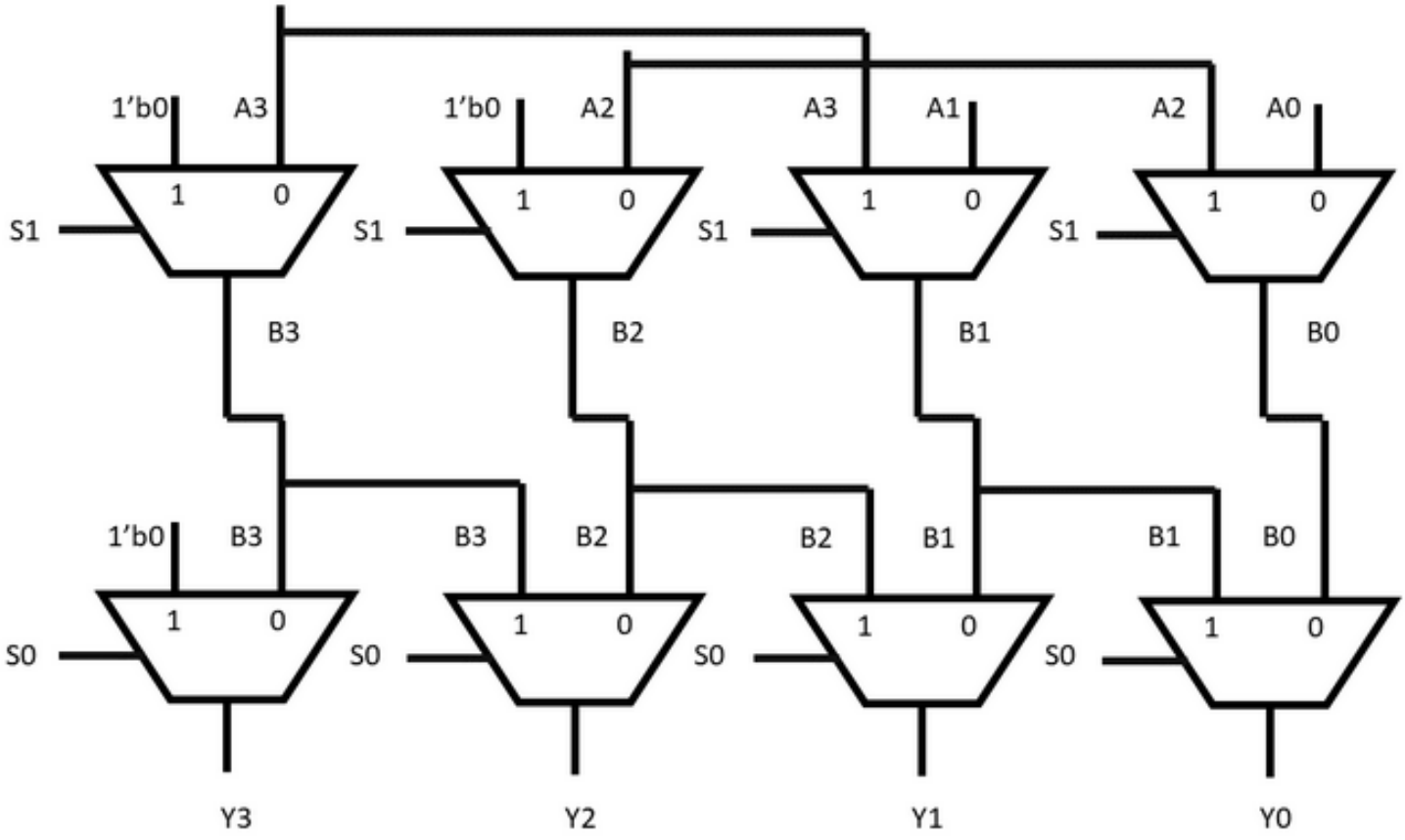


Figure 5.2: Block diagram of barrel right shifter using 2:1 mux

5.3 Application of Barrel Shifter in Binary GCD algorithm

One of the applications of shifters is for determining the Greatest Common Divisor (GCD) of two or more unsigned numbers. Binary GCD algorithm also called Steins' Algorithm or Euclidian Algorithm computes the GCD of non negative numbers using binary shift operations. Left shift and right shift are necessary to find GCD of two unsigned numbers using Steins' algorithm. The steps to find GCD using Steins' algorithm are:

1. If both A and B are 0, then the GCD(A,B) is 0.
2. If B is 0, then the GCD(A,0) is A, and if A is 0, then the GCD(0,B) is B.
3. If both A and B are even, the GCD(A,B) is equal to twice the GCD of A divided by 2 and B divided by 2.

4. If A is even and B is odd, the GCD(A,B) is equal to the GCD of A divided by 2 and B.

5. If A is odd and B is even, the GCD(A,B) is equal to the GCD of A and B divided by 2.

6. If both A and B are odd, the GCD(A,B) is equal to the GCD of the absolute difference between A and B divided by 2, and B.

7. Repeat steps 3-6 until either A equals B or A becomes 0.

As described in the algorithm, multiplication and division by 2 is to be performed which are nothing but left and right shift. The concept is illustrated through an example. Assuming 2 and 4 are the inputs for which GCD needs to be computed. As both the numbers are even, GCD(2,4) is twice the GCD(1,2). For implementing the above step, right shift operation is to be performed to divide 2 and 4 by 2 as depicted in Figure 5.3. The simulated result is shown in Figure **??**. In the next step, because 1 is odd and 2 is even, GCD(1,2) will be GCD(1,1). So GCD of 1,1 is 1. And in the first step, there was a multiplication by 2 which is to be performed in the last step. So we need to multiply GCD(1,1) with 2 which is right shift of 1 depicted in Figure **??** and respective result in Figure 5.6.

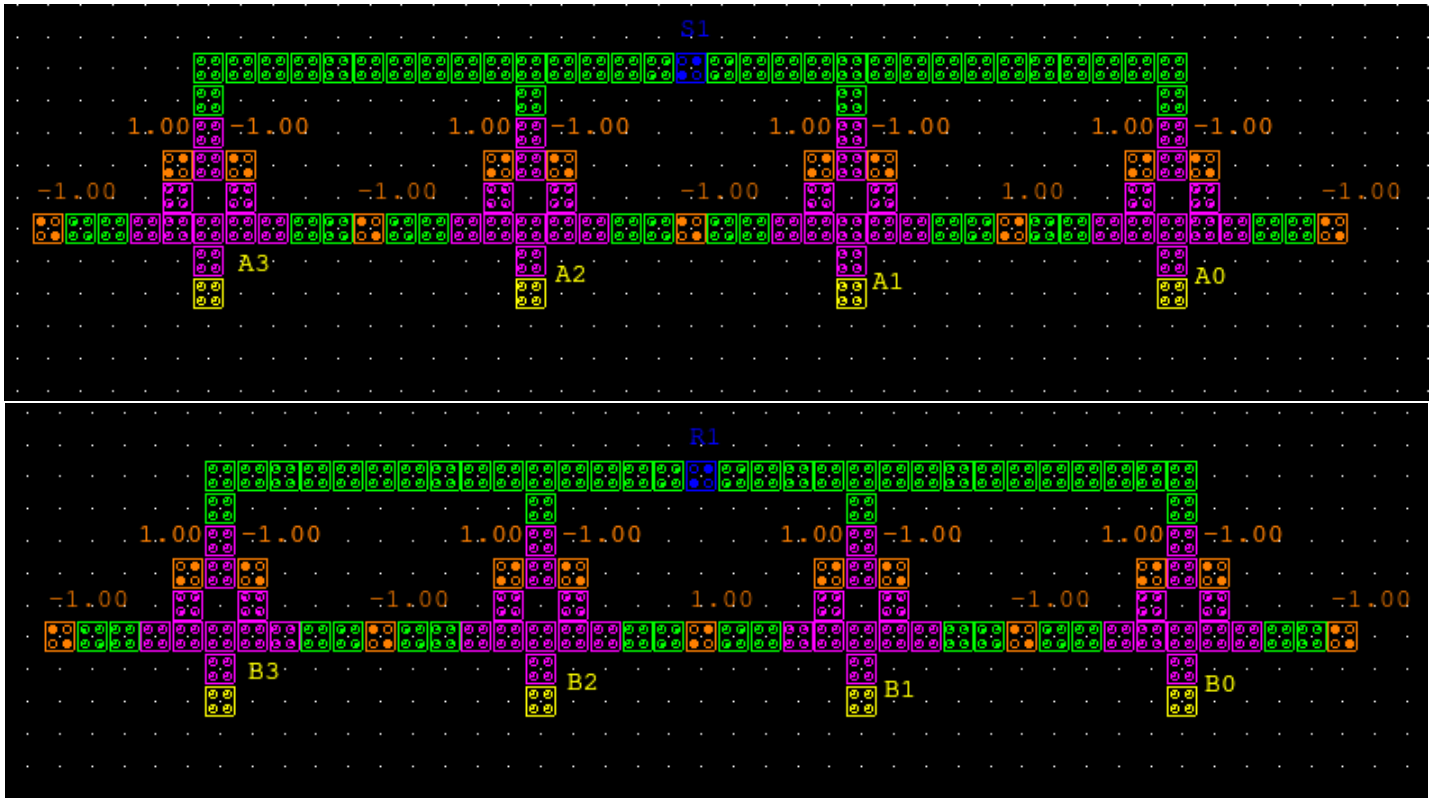


Figure 5.3: Right shift of numbers 2 and 4

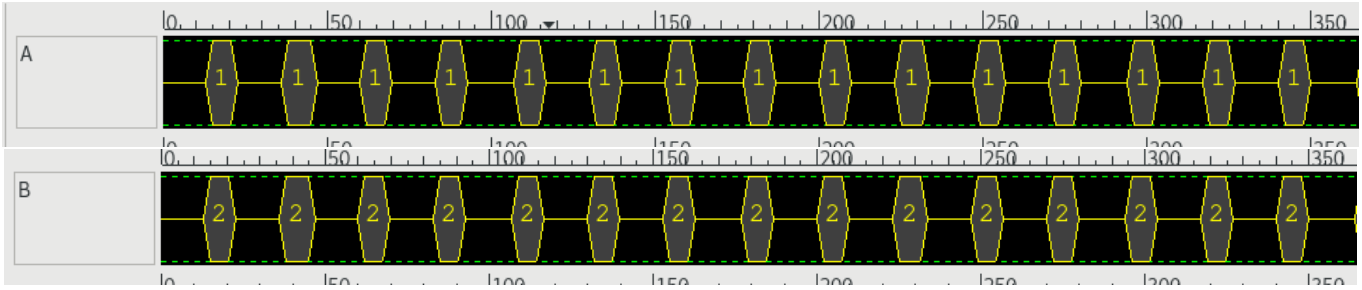


Figure 5.4: Output after right shift of numbers 2 and 4

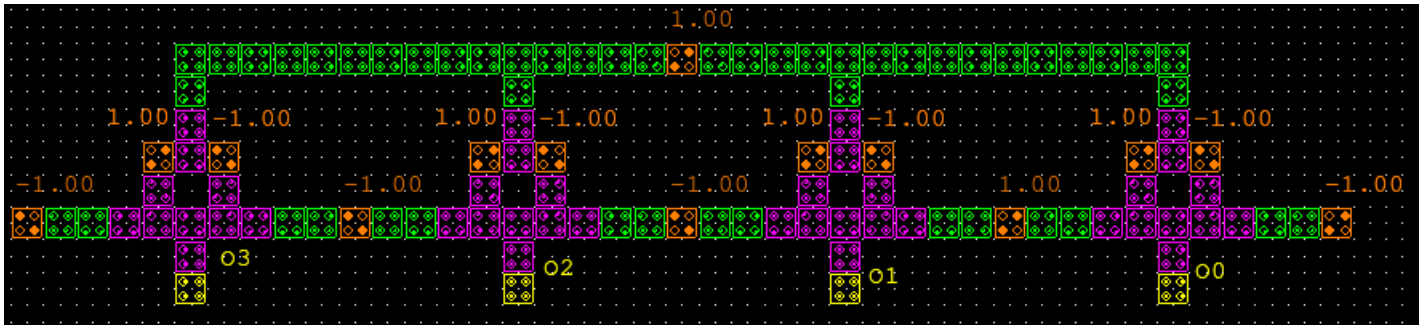


Figure 5.5: Left shift operation of 1

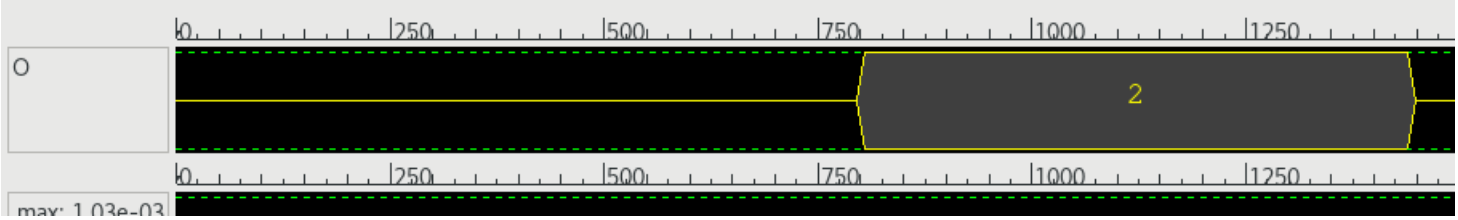


Figure 5.6: Output after left shift operation of 1

5.4 Simulation and Results

Because of the advantages of the mux structure mentioned above, it is used to implement the barrel shifter.The designed QCA structure of the barrel shifter in described in this section. The proposed shifter consists of eight 2:1 multiplexers, a primary input (A3,A2,A1,A0), a control input (S1,S0) and output (Y3,Y2,Y1,Y0). The QCA layout of the proposed shifter is shown in Figure 5.7 and respective simulation results are presented in Figure 5.8. A comparative analysis of the proposed barrel shifter with existing shifter designs is presented in Table 5.2

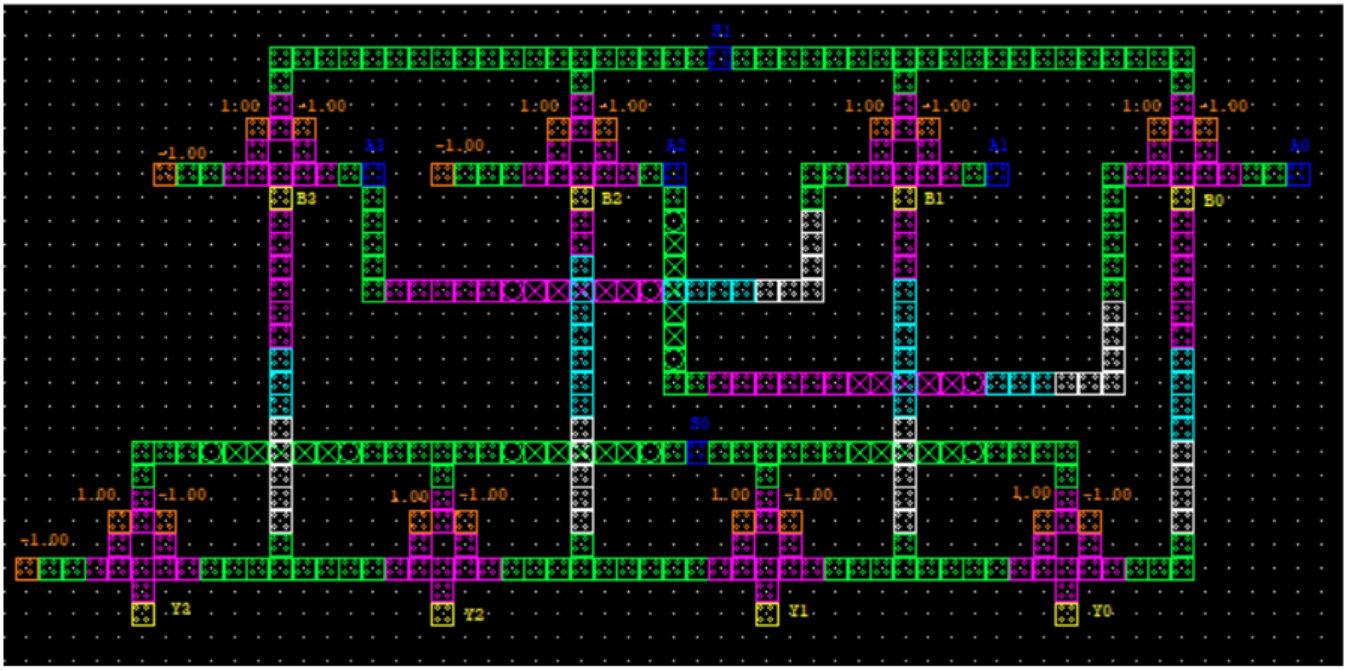


Figure 5.7: QCA layout of the proposed 4-bit barrel right shifter using 2:1 mux

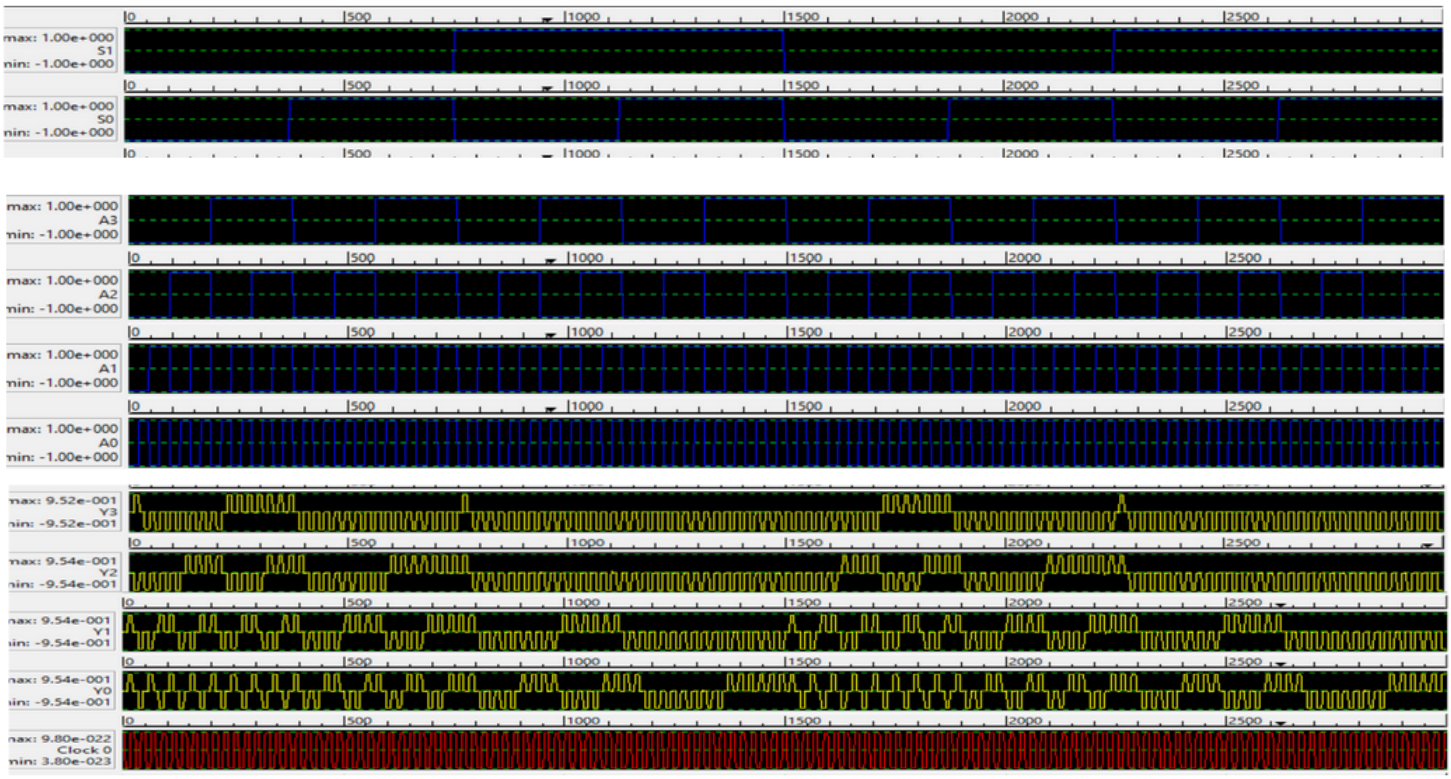


Figure 5.8: Simulation results of proposed barrel shifter

Table 5.2: Comparison of shifters.

Circuit	Cell count	Cell area	Delay
[21]	2021	2.4 μm^2	11
[45]	480	0.5 μm^2	9
Proposed Design	381	0.57 μm^2	6

A comparison was made between the design of Quantum Cellular Automata (QCA) technology and the existing CMOS technology design. QCA technology was found to possess several advantages over CMOS technology, including reduced area, improved speed, and lower power consumption. The specific details of this comparison can be found in Table 5.3.

Table 5.3: Comparison of QCA and CMOS.

Parameter	CMOS [46]	QCA
Area	9.6 μm^2	0.5 μm^2
Power	2400 nW	5.006nW

The QCA design demonstrates higher area efficiency compared to the CMOS design, meaning that it requires less physical space to implement. Furthermore, the power dissipation of the QCA design is relatively low , indicating reduced energy consumption compared to CMOS.

CHAPTER 6
Conclusion and Future Scope

This thesis proposes the design 4- bit barrel shifter using 2:1 multiplexer in QCA technology. To start with, the fundamental principles of QCA design that includes QCA builiding blocks, clocking schemes and wire crossings are presented in this work. The research focuses on the design of an optimized 4-bit barrel shifter. The proposed structure has a cell count of 381. It occupies an area of $0.57\mu m^2$.The power dissipation of the proposed design is 2.35e-002eV. It has been found that the design is more efficient in terms of area and power dissipation compared to existing shifter designs. The operation is verified by QCADesigner E tool. Further, the application of barrel shifters in the computation of GCD of numbers is also explored.

This work can be extended to include self checking mechanisms to implement a fault tolerant design in QCA technology. In addition, designing a testable architecture of barrel shifters in QCA can also done.

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